IEEE CAS Society • AICAS 2026 Satellite Workshop

IEEE Chiplet Workshop 2026

Circuits and Systems for Next-Generation AI Computing (CSNAIC)

AICAS 2026 • Ha Long Bay, Vietnam • 18 Sep 2026 • Shanghai, China • 9 Oct 2026

Workshop Overview

The 2nd IEEE Chiplet Workshop on Circuits and Systems for Next-Generation AI Computing (CSNAIC) is a satellite event of AICAS 2026, sponsored by the IEEE Circuits and Systems Society (CASS). This year features a dual-venue format: Ha Long Bay, Vietnam on 18 September 2026 (co-located with AICAS 2026), and Shanghai, China on 9 October 2026.

The workshop brings together researchers and industry experts to discuss emerging challenges and innovative solutions in chiplet-based architectures, advanced circuits and systems, and EDA technologies for next-generation AI computing.

Topics of Interest

- Chiplet architectures and 2.5D/3D integration
- High-speed interconnects and advanced packaging
- Compute-in-memory and near-memory computing
- Heterogeneous AI accelerator design
- Reconfigurable and low-power edge AI systems
- EDA methodologies for chiplet-based systems
- Standardization for scalable chiplet ecosystems

Workshop Highlights

- Five invited talks by leading international researchers
- Dual-venue format: Vietnam (AICAS) + Shanghai
- Poster Session & Call for Papers at Shanghai
- Sponsored by IEEE Circuits and Systems Society
- Networking with academia and industry experts

Organizing Committee

Workshop Co-Chairs Chixiao Chen, Fudan University
Anh Tuan Do, A*STAR, Singapore

Technical Program

18 Sep 2026 1:30 - 5:00 PM | Ha Long Bay, Vietnam

1:30 - 1:40	Opening Remarks
1:40 - 2:25	TBD *Tulika Mitra (National University of Singapore) (Tentative)*
2:25 - 3:10	Scalable 3D Compute-in/near-Memory Systems with Reusable Active Interposer *Chixiao Chen (Fudan University)*
3:10 - 3:25	Coffee Break
3:25 - 4:10	Low-Power Wireline/Optical Transceivers for Next-Generation AI Applications *Quan Pan (Southern University of Science and Technology)*
4:10 - 4:55	Progress on Crosstalk Cancellation Techniques for High-Speed Parallel Interconnects *Yuan Du (Nanjing University)*
4:55 - 5:40	A 16Gb/s/pin 0.51pJ/bit Single-Ended NRZ Transceiver with VDDQ Ripple Compensation for Memory Interfaces *Wenning Jiang (Fudan University)*

Shanghai Session (9 October 2026)

The Shanghai session will be held on 9 October 2026 at Fudan University, featuring invited talks, a poster session with call-for-papers, and industry panel discussions.

Official website: https://2026.iccconf.cn/ieee

Call for Papers (Shanghai Session)

We invite original contributions on chiplet circuits, architectures, and systems for the Shanghai session poster presentation.

Submission format: 1-page poster-style PDF
Submission portal: EasyChair (ICW 2026)
Contact: secretary.chiplet.workshop@gmail.com

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